CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended): An improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled by a microprocessor, the improvement which comprises:

writing the digital data of a given data frame from the first data bus to a memory having a settable size;

informing the microprocessor, in a form of an interrupt signal generated by a memory control unit, if the memory is full or if the memory contains an entry indicating an end of a respective data frame ~~has been reached~~;

determining via the microprocessor from the memory control unit a quantity of the digital data to be read from the memory;

reading via the microprocessor the digital data from the memory;

setting via the microprocessor a size of the memory <u>for a following writing procedure in said memory</u>; and

transmitting from the microprocessor to the memory control unit an acknowledgment of a reception of ~~a~~ <u>the</u> data <u>being read out from the memory</u> ~~block of the digital data~~.

2 (original): The method according to claim 1, which comprises supplying the digital data from the first data bus to a high-level data link control logic unit which checks whether the digital data has been received correctly before the digital data is written to the memory.

3 (currently amended): An improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to the first data bus, the improvement which comprises:

writing the digital data from the first data bus to a memory having a settable size;

performing one of informing the microprocessor, in a form of an interrupt generated by a memory control unit, if the memory is ready to accept new data from the first data bus, and the microprocessor asking the memory control unit if the memory is ready to accept the new data from the first data bus;

writing via the microprocessor the new data to the memory;

setting via the microprocessor a size of the memory for a following writing procedure in said memory;

transmitting from the microprocessor to the memory control unit an acknowledgment of the data being written into the memory ~~an end of transmission of the new data~~; and

placing the new data onto the second data bus.

4 (original): The method according to claim 3, which comprises supplying the new data to a high-level data link control logic unit before it is placed onto the second data

bus, the high-level data link control logic unit adding error-checking data to the new data.

5 (currently amended): A configuration for performing an ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable length from a first data bus to a second data bus operated asynchronously with respect to the first data bus and controlled ~~and read by~~ a microprocessor, the configuration comprising:

a memory having a variable size for storing data received from the first data bus and for subsequently reading out by the microprocessor;

a control device for controlling access operations to said memory by the first data bus and the microprocessor;

a first register storing an amount of the data being currently written in the memory and read out from the microprocessor ~~a value representing a present size of said memory, said value being variable in each read cycle of the microprocessor~~; and

a second register storing, for a following writing procedure, a present size of memory, said second register having a

content selectively modifiable with each read cycle of the microprocessor ~~a quantity of the data just written to said memory~~.

6 (original): The configuration according to claim 5, including a high-level data link control HDLC logic unit connected between the first data bus and said memory.